WHAT IS CLAIMEDIS:

1. A bit rate-independent optical receiver, comprising:

an opto-electric converter for converting an input optical signal into an electric signal;

an amplifier circuit for amplifying the electrical signal;

a bit rate-sensing circuit connected to receive the amplified electrical signal for generating a sensing signal with a voltage level determined on the basis of a bit rate of the electrical signal;

a bit rate-recognition circuit for generating a recognition signal that is further amplified from the sensing signal, said bit rate-recognition circuit having a structure of providing an extended range of recognizable total input voltages by connecting a plurality of logarithm amplifiers in series, each of which logarithm amplifiers has a predetermined range of recognizable input voltage;

a clock/data recovery circuit for reproducing a clock signal and data from the amplified electrical signal in accordance with a control signal and outputting the reproduced clock signal and data; and,

a controller for determining a bit rate corresponding to a voltage level of the recognition signal by referring to a look-up table defining a predetermined relationship of the bit rate to the voltage level, and for providing the clock/data recovery circuit with the control signal representative of the bit rate.

2. The optical receiver of claim 1, wherein the amplifier circuit further comprises a low-noise amplifier for eliminating noise from the electrical signal outputted from the opto-electric converter and for amplifying the noise-free electrical signal by a given amplification factor; and, a limiting amplifier for re-amplifying the amplified electrical signal within a predetermined voltage level.

3. The optical receiver of claim 1, wherein the bit rate-recognition circuit further comprises:

a plurality of the logarithm amplifiers connected to sequentially amplify the sensing signal outputted from the bit rate-sensing circuit;

a plurality of rectifiers respectively connected to one input of the respective logarithm amplifiers and to one output of at least one said logarithm amplifier, for rectifying the sensing signal inputted thereto; and,

an adder connected to provide the sum of output signals of the plurality of rectifiers.

4. The optical receiver of claim 1, wherein the clock/data recovery circuit further comprises:

a phase-locked loop circuit for generating a reference clock signal in accordance with the control circuit provided by the controller; and,

at least one flip-flop connected to reproduce a clock signal and data, in accordance with the reference clock signal, from the amplified electrical signal supplied from the amplifier circuit.

5. The optical receiver of claim 4, wherein the phase-locked loop circuit further comprises:

a phase comparator for comparing a frequency and a phase of the amplified electrical signal outputted from the amplifier circuit with those of the reference clock signal and consequently providing an error voltage according to the comparison;

a loop filter for filtering the error voltage outputted from the phase comparator and providing the filtered error voltage; and,

a voltage controlled oscillator for generating the corresponding reference clock signal on the basis of the error voltage of the loop filter and the control signal for oscillation of the controller.

6. The optical receiver of claim 1, wherein the controller comprises a memory for storing a look-up table indicating a predetermined data set of the bit rate to the voltage level.